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Technical Note

A contact resistance model for scanning probe phase-change memory

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Abstract

A novel mechanical model was proposed to calculate the contact resistance at tip and capping layer interface for scanning probe phase-change memory applications. The resulting I-V curve calculated from this model that combines Hertzian contact theory with the Schottky diode effect has exhibited a good agreement with the experimental measurements under the same system architecture. The role of contact resistance on the write efficacy of scanning probe phase-change memory was also evaluated by introducing the calculated contact resistance into the previous electrothermal simulations for cases of writing crystalline bits in amorphous starting phase and writing amorphous bits in crystalline starting phase. The consequent written marks and I-V curve show a closer match with the experimental observation compared to the case without including contact resistance.

Keywords: contact resistance, phase-change media, scanning probe, model, Schottky diode

(Some figures may appear in colour only in the online journal)

1. Introduction

Global digital data is currently increasing at an unprecedented rate due to the recent progress achieved in information technology (IT), which is much faster than the growth rate of the storage capacity for conventional storage devices such as magnetic hard disks and Flash memory [1–3]. In order to outperform the pace of digital data, one possible approach is to store ever-increasing amounts of data in ever-decreasing dimensions of storage devices through the development of microelectronic packaging technologies such as system-onchip (SOC), multi-chip module (MCM), system-in-package (SIP), and system-on-package (SOP) [4, 5]. Such acceleration on higher package density obviously triggers the requirement for more advanced wafer level integrated circuit (IC) testing

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that is performed to examine the testing and validation of the circuits at the wafer level. Today, probe cards are commonly used in wafer level IC testing as an interface between an electronic test system and a semiconductor wafer so as to provide an electrical path between them. The microelectromechanical systems (MEMS) based probe card has recently gained more attention than its compatriot due to its better compatibility with present IC technology and its lower cost for fabricating high-density probe arrays [4, 6]. In the MEMS based probe card, test current that flows between a probe and an electrical pad on the wafer employed to give an electrical/mechanical interface between pin packaging and the signal lines in the die, is constricted to the intermetallic contact areas. Therefore, the contact resistance across this interface would dramatically affect the integrity of the test signal and may disadvantageously result in false device failure identification if it is not carefully exercised.

In addition to MEMS probe card, contact resistance also plays an important role in determining the performance of



Figure 1. Schematic of scanning probe phase-change memory in two-dimension (2D). Cylindrical symmetry is assumed.

scanning probe phase-change memory regarded as one of the most promising candidates for next generation data storage device [7], as shown in figure 1.

In scanning probe phase-change memory, recording is accomplished by applying suitable voltage pulse via a conductive tip into a phase-change layer whose phase can be switched between highly resistive amorphous state and highly conductive crystalline state through Joule heating, while replay can be realized by detecting the change in electrical resistivity between crystalline and amorphous region through a readout potential. At present, scanning probe phase-change memory has been considered as one of the promising candidates for next-generation mass storage devices due to its ultra-high density, fast data rate, and low power consumption, and thus received considerable attention from both experimental and theoretical points of view [8-17]. However, to the authors' knowledge, none of the already existing theoretical models for scanning probe phase-change memory has seriously taken into account the contact resistance at the interface between tip and capping layer that is usually adopted to protect phase-change layer from wear and corrosion. In practice, when the probe system is subjected to a writing voltage pulse, an electrical potential difference between tip and capping layer will take place, and thus give rise to a current to flow them to generate the contact resistance. It is obvious that the advent of contact resistance would change the whole system resistance as well as the Joule heating generated inside the phase-change layer, which can finally have a pronounced influence on the phase transformation behavior of the recording media.

Several analytical and numerical models that investigate the contact mechanics at the interface between the probe and sample have so far been proposed. Kwak *et al* investigated theoretically the influence of various tip shapes on the contact resistance when contacting with rough surfaces using the Johnson–Kendall–Roberts (JKR) theory [18–20]. It should be however noted that the JKR model is only suitable for compliant solids, while the practicality of applying JKR theory to capping layer with good mechanical hardness that is usually required by scanning probe phase-change memory is not ensured yet. The contact mechanics between atomic force microscopy and non-polar molecular monolayer was evaluated



Figure 2. Schematic of tip-sample interface for a loading force.

by Nikogeorgos et al based on the Derjaguin-Muller-Toporov (DMT) theory [20–22]. Similar to the previous case, in spite of the wide application of DMT model on organic materials, its suitability for modeling contact mechanics in scanning probe phase-change memory still remain uncertain. Bora et al developed a numerical contact model using degrees of freedom normal to the surface and the Boussinesq solution to relate the normal load to the long-range surface displacement response [23]. Nevertheless, a rough surface was assumed in their model rather than a flat surface usually needed for scanning probe phase-change memory. Considering the limits of the above models, the requirement to develop a more physical based model to calculate the tip-capping layer contact resistance so as to more closely mimic the practical setup, and thus to provide a better scenario for system optimization becomes very necessary.

2. Model techniques

The contact interface between a smooth tip and a smooth flat sample surface with an application of a loading force is schematically shown in figure 2.

This applied loading force will obviously cause a deformation in the shapes of the tip and sample. Deformation can be generally classified into elastic deformation that is recoverable after removal of loading force and plastic deformation that is irremovable after retreating the loading force. As the permanent tip deformation was not observed in previous experiments [24], the tip deformation considered here is assumed to be elastic. According to Hertzian contact theory [25], the indentation, H_{defl} , can be written as a function of the radius (*r*) of curvature at the apex of the tip, and the loading force *F*, given by [26]:

$$H_{\rm defl} = \left(\frac{9F^2}{16rE^{*2}}\right)^{\frac{1}{3}},\tag{1}$$

where E^* is the equivalent Young's modulus of elasticity, defined as [26]:

$$\frac{1}{E^*} = \frac{1 - \nu_1^2}{E_1} + \frac{1 - \nu_2^2}{E_2},\tag{2}$$

where E_1 and E_2 are the elastic modulus of the tip and the sample, respectively, and v_1 , v_2 are the corresponding Poisson's ratios. In this case, the contact area radius for a Hertz elastic contact under a given force, r_{con} is calculated by:

$$r_{\rm con} = \left(r^2 - \left(r - H_{\rm defl}^{\frac{1}{3}}\right)^2\right)^{\frac{1}{2}}.$$
 (3)



Figure 3. Geometry of tip–sample system used for experiment and simulation.

Alternatively, the contact radius can be written as [25, 27]:

$$r_{\rm con} = \left(\frac{3Fr}{4E^*}\right)^{\frac{1}{3}}.$$
 (4)

It should be noticed that equation (3) is equivalent to equation (4) at nanoscale dimensions, due to the fact that deflection caused by pushing the tip down into the sample only occurs at the contact point at tip–sample interface rather than the rest of the sample surface [26, 28, 29] due to the relatively small loading force. In addition, the contact radius in equation (3) is described as a function of the tip indentation in comparison with equation (4). As tip indentation may change the actual distance between tip and phase-change layer and thus modify the whole system resistance, the dependence of contact radius on tip indentation on contact resistance, thereby essential for the optimization of system performance. Considering the aforementioned factors, the contact radius in this note is chosen to be written in the form of equation (3).

The contact resistance can thus be estimated as a function of the contact surface resistivities and the radius of the contact area, resulting in [30]:

$$R_{\rm contact} = \frac{\rho_{\rm tip} + \rho_{\rm sample}}{4r_{\rm con}},\tag{5}$$

where ρ_{tip} and ρ_{sample} are the resistivity of the tip and sample, respectively.

The mechanical model introduced above allows for the estimate of contact resistance when tip is brought into close proximity to the sample provided that tip loading force and tip apex radius are already known. In order to verify the physical reality of this model, the contact resistance for a PtSi tip and traditional Si tip that scan over the surface of an Au sample (note that the phase-change media stack is not included in this case) were calculated, and the resulting I-V curve was subsequently compared with the experimental counterpart [24]. The stack system deployed for both experiment and simulation is schematically illustrated in figure 3.

As can be seen from figure 3, the resistance determined by an I-V curve is not just contact resistance, but also a summation of cantilever resistance, tip resistance, and sample spreading resistance. Therefore, the total measured resistance can be



Figure 4. Geometry of PtSi apex for resistance calculation.

expressed by:

$$R_{\text{measure}} = R_{\text{cantilever}} + R_{\text{tip}} + R_{\text{sample}} + R_{\text{contact}}$$
$$= \rho_{\text{cantilever}} \frac{L}{Wt} + R_{\text{tip}} + \frac{\rho_{\text{Au}}}{2d} + R_{\text{contact}}, \tag{6}$$

where $\rho_{\text{cantilever}}$ and ρ_{Au} are the resistivities of the cantilever (Si in this case) and Au sample, respectively, and *d* is the physical diameter of the tip bottom area. R_{tip} can be mathematically calculated through:

$$R_{\rm tip} = R_{\rm Si} + R_{\rm PtSi}.$$
 (7)

 R_{PtSi} can be calculated through the integration of the resistance of an infinitesimally small cylinder over H_{PtSi} , as shown in figure 4.

The resistance of such a cylinder is given by:

$$R_{\text{cylinder}} = \frac{4\rho_{\text{PtSi}} \, dh}{\pi \, d_{\text{cylinder}}^2},\tag{8}$$

where dh is the height of the cylinder, and $d_{cylinder}$ is the diameter of the cylinder.

According to homothetic triangle theory, $d_{cylinder}$ can be described by:

$$d_{\text{cylinder}} = d + \frac{h(D_{\text{interface}} - d)}{H_{\text{PtSi}}},$$
(9)

Substituting equation (9) into equation (8) and integrating equation (8) over the height of PtSi apex, equation (10) is obtained:

$$R_{\text{cylinder}} = \int_0^{H_{\text{PtSi}}} \frac{4\rho_{\text{PtSi}} \, dh}{\pi \left(d + \frac{h(D_{\text{interface}} - d)}{H_{\text{PtSi}}}\right)^2}.$$
 (10)

After mathematical integration, the final form of R_{PtSi} is written as:

$$R_{\text{PtSi}} = \frac{H_{\text{PtSi}}^2 \rho_{\text{PtSi}}}{\pi \left(\frac{D_{\text{interface}} - d}{2}\right) \left(\frac{dH_{\text{PtSi}}}{2}\right)} - \frac{H_{\text{PtSi}}^2 \rho_{\text{PtSi}}}{\pi \left(\frac{D_{\text{interface}} - d}{2}\right) \left(\frac{D_{\text{interface}} H_{\text{PtSi}}}{2}\right)}.$$
(11)

 R_{Si} can be calculated in a similar manner to R_{PtSi} introduced above, thereby given by:

$$R_{\rm Si} = \frac{H_{\rm Si}^2 \rho_{\rm Si}}{\pi \left(\frac{D-D_{\rm interface}}{2}\right) \left(\frac{D_{\rm interface}H_{\rm Si}}{2}\right)} - \frac{H_{\rm Si}^2 \rho_{\rm Si}}{\pi \left(\frac{D-D_{\rm interface}}{2}\right) \left(\frac{DH_{\rm Si}}{2}\right)},\tag{12}$$

where the physical meaning of the geometry parameters and the corresponding values can be obtained from figure 3. It should be also kept in mind that the resulting I-V curves may not simply obey the Ohm's law but exhibits an exponential



Figure 5. Resulting I-V curves for both PtSi tip and SI tip. The experimental I-V curves were adapted from [24]. The loading forces for PtSi tip and Si tip are 56 and 500 nN, respectively. The effective Young's modulus is estimated to be 62.6 GPa.

increase due to the formation of metal-semiconductor contact between tip and sample that behaves like a diode, known as the Schottky effect [31]. Therefore, the influence of the Schottky diode on the current flowing through the system can be described as [32]:

$$I_D = I_0 \cdot \left(\exp\left(\frac{qV_{\text{diode}} - qI_D R_{\text{contact}}}{nkT}\right) - 1 \right), \qquad (13)$$

where I_0 is a constant with a value of $2 \cdot 10^{-11}$ A [33] that is related to the Schottky barrier height; V_{diode} is the voltage across the diode; *n* is a constant with a value of 1 and I_D is the current that flows through the system. As a result, the corresponding I-V data can be obtained by simultaneously solving equations (13) and (14) defined as follows:

$$I_D = (V_{\text{applied}} - V_{\text{diode}}) / (R_{\text{cantilever}} + R_{\text{tip}} + R_{\text{contact}} + R_{\text{Au}}),$$
(14)

where V_{applied} is the electrical potential between cantilever and sample.

3. Results and discussions

The comparison between the calculated I-V curves and the experimentally measured one, as shown in figure 5, has demonstrated the ability to accurately estimate the contact resistance using such a mechanical model, as the calculated I-V curves display a good match with the corresponding measurements.

It is therefore informative to introduce this mechanical model into the previous electrothermal simulation to evaluate the role of contact resistance between tip and sample (capping layer in this case) on the writing efficacy of scanning probe phase-change memory, resulting in figure 6.

The phase-change media stack adopted here for both the experiment and simulation consists of a 20 nm recording layer sandwiched between a 6 nm N_2 doped carbon capping layer and 120 nm N_2 doped carbon underlayer, deposited on top of a Si substrate. The ability to experimentally write crystalline bits using such a media stack is illustrated in figure 6(*a*) [16],

exhibiting crystalline marks with average diameter of 50 nm by a 4 V pulse of 100 μ s. The corresponding simulated bit with a diameter of approximately 64 nm that was obtained from the previous electrothermal simulation by simultaneously solving the Laplace equation, the heat transfer equation, and the JMAK equation [8, 11, 12] but with the exclusion of tip-capping layer contact resistance is depicted in figure 6(b). The difference on the mark diameter between figures 6(a) and (b) may arise from the neglect of the tip-capping layer contact resistance, which would decrease the whole system resistance, and thus generate larger writing current and more Joule heating inside the recording layer. However, the introduction of tip-capping layer contact resistance into the previous electrothermal model results in a simulated bit with a diameter of around 50 nm shown in figure 6(c), which fits well to experimental finding. According to equation (5), the value of the contact resistance calculated for figure 6(c) is approximately 80 k Ω for a tip force of 300 nN (typical for that applied during writing) and for $\rho_{\text{sample}} = 6 \times 10^{-3} \ \Omega \text{m}$ (in our case sample is the capping layer) and $\rho_{\rm tip}$ = 0.3 $\,\times\,$ 10^{-6} $\Omega{\rm m}$ with an effective Young's modulus of 20.2 GPa [34]. The physical reality of this proposed mechanical model can be further verified through the comparison between the experimental I-V curve in figure 6(a) and the simulated curve in figure 6(c), as shown in figure 7. It is clearly observed that incorporating the previous electrothermal model with the calculated contact resistance exhibits a similar maximum magnitude of the resulting current and a slightly smaller threshold voltage as compared to the experimental one. It should also be noted that it is difficult to reproduce exactly the same I-V curve, as reported by the real experiment, most probably due to uncertainty in the values of the resistivity of the under layer. Underestimating this value in the model could increase the value of the electrical field, thus slightly lowering the threshold voltage. Nevertheless, even with such an uncertainty the developed model is still able to well approach the experimental observation. Therefore, the reported comparisons presented above clearly indicates that the tip-capping layer contact resistance plays a critical role on determining the whole system resistance and thus can influence written mark size and the writing current for a given write pulse, thereby necessitating the inclusion of the contact resistance effect into the theoretical model for scanning probe phase-change material so as to more closely simulate the practical environment.

The effect of the contact resistance on the diameter of the resulting bits is theoretically evaluated by integrating the previous electrothermal model with this newly developed mechanical model, resulting in figure 8. It can be seen that the diameter of the written bit is gradually reduced along with the increase of the contact resistance. This is expected since the larger contact resistance would increase the whole system resistance and thus further reduce the writing current for a given voltage pulse. In addition, the bit diameter exhibits a non-linear dependence on the contact resistance, which can be ascribed to the non-linear resistivity of the phase-change layer itself that strongly replies on the temperature and electric field [35].

It is necessary to point out that in conventional phasechange storage devices, including phase-change optical disks



Figure 6. The generated crystalline bit using a typical media stack (see [16]) from (*a*) experiment, (*b*) simulation with exclusion of contact resistance, and (*c*) simulation with inclusion of contact resistance. The experimental current image was adapted from [16], and the characteristic parameters for simulations can be found in [8] and [12].



Figure 7. The *I*–*V* characteristic comparison between the experiment (figure 6(a)) and the simulation with the introduction of contact resistance (figure 6(c)). The experimental *I*–*V* curve is taken from [16].

and PCRAM devices, the recording process is actually operated by writing amorphous bits into the crystalline starting phase. The experimental writing of amorphous bits using scanning probe phase-change memory has been previously realized only by Tanaka's group which immersed phasechange layer in an inert liquid to protect it from oxidation [36]. Obviously a liquid protective layer is not practicable for real storage systems. In this case, the capability of writing amorphous bits using scanning probe phase-change memory was evaluated here by means of the previously developed amorphization approach [8] with the introduction of contact resistance into the tip-capping layer interface, giving rise to figure 9.

Note that amorphization can be achieved by heating the crystalline starting phase to the melting temperature (around 630 $^{\circ}$ C [8]), followed by a rapid cooling. As can be seen from figure 9, both cases reveal a formation of amorphous bits with semi-ellipsoidal shape growing from the top portion



Figure 8. Dependence of bit diameter on contact resistance. The phase-change media stack and the characteristic parameters used in the simulation are as for figure 6.

of the phase-change layer where the melting temperature has been approached, coinciding with the previous findings. In addition, the amorphous bit without the introduction of contact resistance exhibits a larger vertical depth than the case without contact resistance. This is expected since the writing current stemming from the model with contact resistance is obviously smaller than that without contact resistance for a given pulse. In this case, the bottom region of the phase-change layer can not be sufficiently heated to the melting temperature due to the heat dissipation toward the substrate, thus remaining in crystalline phase. Figure 9 clearly indicates that similar to the crystallization case, contact resistance also has a significant impact on the resulting amorphous bit size, and thereby needs to be taken into account for the future analysis in order to more accurately describe the amorphization behavior of phasechange materials.



Figure 9. The amorphous bits written by a 5 V pulse of 100 μ s using the phase-change probe system for figure 6 for the cases (*a*) without contact resistance and (*b*) with contact resistance. The parameters used for calculating contact resistance are as for figure 6.

4. Conclusions

A novel mechanical model that allows for the calculation of tip-capping layer contact resistance for scanning probe phasechange memory was described. The consequent I-V curves and the written crystalline marks from the combination of the previous crystallization model with this newly developed mechanical model exhibits a good match with the experimental counterparts, thus demonstrating its physical reality as well as the important extent of the contact resistance to the writing of crystalline bits using scanning probe phase-change memory. The capability of writing amorphous bits using scanning probe phase-change memory was also assessed by consolidating the previous amorphization model with the calculated contact resistance. It is found that the tip-capping layer contact resistance has a significant influence on the resulting amorphous bit size due to the variation of the writing current.

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References

- Park K-S, Park Y-P and Park N-C 2011 IEEE Trans. Magn. 47 539
- [2] Iwasaki I 2012 J. Magn. Magn. Mater. 324 244
- [3] Fontana R E, Hetzler S R and Decad G 2012 *IEEE Trans.* Magn. 48 1692
- [4] Wang F, Li X X and Feng S L 2008 J. Micromech. Microeng. 18 055008
- [5] Tummala R 2006 IEEE Spectr. 43 44
- [6] Wang F, Li X X and Feng S L 2009 IEEE Trans. Adv. Packag. 32 468
- [7] Wright C D, Aziz M M, Shah P and Wang L 2011 Curr. Appl. Phys. 11 e104
- [8] Wright C D, Armand M and Aziz M M 2006 IEEE Trans. Nanotechnol. 5 50
- [9] Aziz M M and Wright C D 2006 J. Appl. Phys. 90 034301

- [10] Wright C D, Shah P, Wang L, Aziz M M, Sebastian A and Pozidis H 2010 Appl. Phys. Lett. 97 173104
- Wang L, Wright C D, Shah P, Aziz M M, Sebastian A, Pozidis H and Pauza A 2011 Japan. J. Appl. Phys. 50 09MD04
- Wright C D, Wang L, Shah P, Aziz M M, Varesi E, Bez R, Moroni M and Cazzaniga F 2011 *IEEE Trans. Nanotechnol.* 10 900
- [13] Kim H J, Choi S K, Kang S H and Oh K H 2007 Appl. Phys. Lett. 90 083103
- [14] Tanaka K 2007 J. Non-Cryst. Solids 353 1899
- [15] Gidon S, Lemonnier O, Rolland B, Bichet O and Dressler O 2004 Appl. Phys. Lett. 85 6392
- [16] Bhaskaran H, Sebastian A, Pauza A, Pozidis H and Despont M 2009 Rev. Sci. Instrum. 80 083701
- [17] Liu Y B, Zhang T, Liu X M, Song Z T, Min G Q, Zhang J, Zhou W M, Wan Y Z, Zhang J P and Feng S L 2009 J. Semicond. **30** 063003
- [18] Kwak J S and Kim T W 2013 J. Adhes. Sci. Technol. 27 1755
- [19] Johnson K L, Kendall K and Roberts A D 1971 Proc. R. Soc. Lond. 324 301
- [20] Bhushan B 1999 Principles and Applications of Tribology (New York: Wiley)
- [21] Nikogeorgos N and Leggett G 2013 J. Tribol. Lett. 50 145
- [22] Derjaguin B V, Muller V M and Toporov Y P 1975 J. Colloid Interface Sci. 53 314
- [23] Bora C K, Plesha M E and Carpick R W 2013 Tribol. Lett. 50 331
- [24] Bhaskaran H, Sebastian A and Despont M 2009 IEEE Trans. Nanotechnol. 8 128
- [25] Johnson K L 1985 Contact Mechanics (Cambridge: Cambridge University Press)
- [26] Lo H and Bain J A 2008 Proc. Symp. on Micro/Nanoscale Heat Transfer (Taiwan) p 1
- [27] Pruitt B L, Park W-T and Kenny T W 2004 J. Microelectromech. Syst. 13 220
- [28] Shi L and Majumdar A 2002 J. Heat Transfer 124 329
- [29] Rahmat M and Hubert P 2010 J. Phys. Chem. C 114 15029
- [30] Bhushan B 2005 Wear 259 1507
- [31] Pierret R F 1996 Semiconductor Device Fundamentals (Boston, MA: Addison-Wesley)
- [32] Cahoon C 2008 *MSc Thesis* Department of Electrical Engineering, Boise State University, ID, USA
- [33] Sedra A S and Smith K C 1998 *Microelectronic Circuits* (Oxford: Oxford University Press)
- [34] Cho S, Chasiotis I, Friedmann T A and Sullivan J P 2005 J. Micromech. Microeng. 15 728
- [35] Ielmini D and Zhang Y-G 2007 J. Appl. Phys. 102 054517
- [36] Satoh H, Sugawara K and Tanaka K 2006 J. Appl. Phys. 99 024306